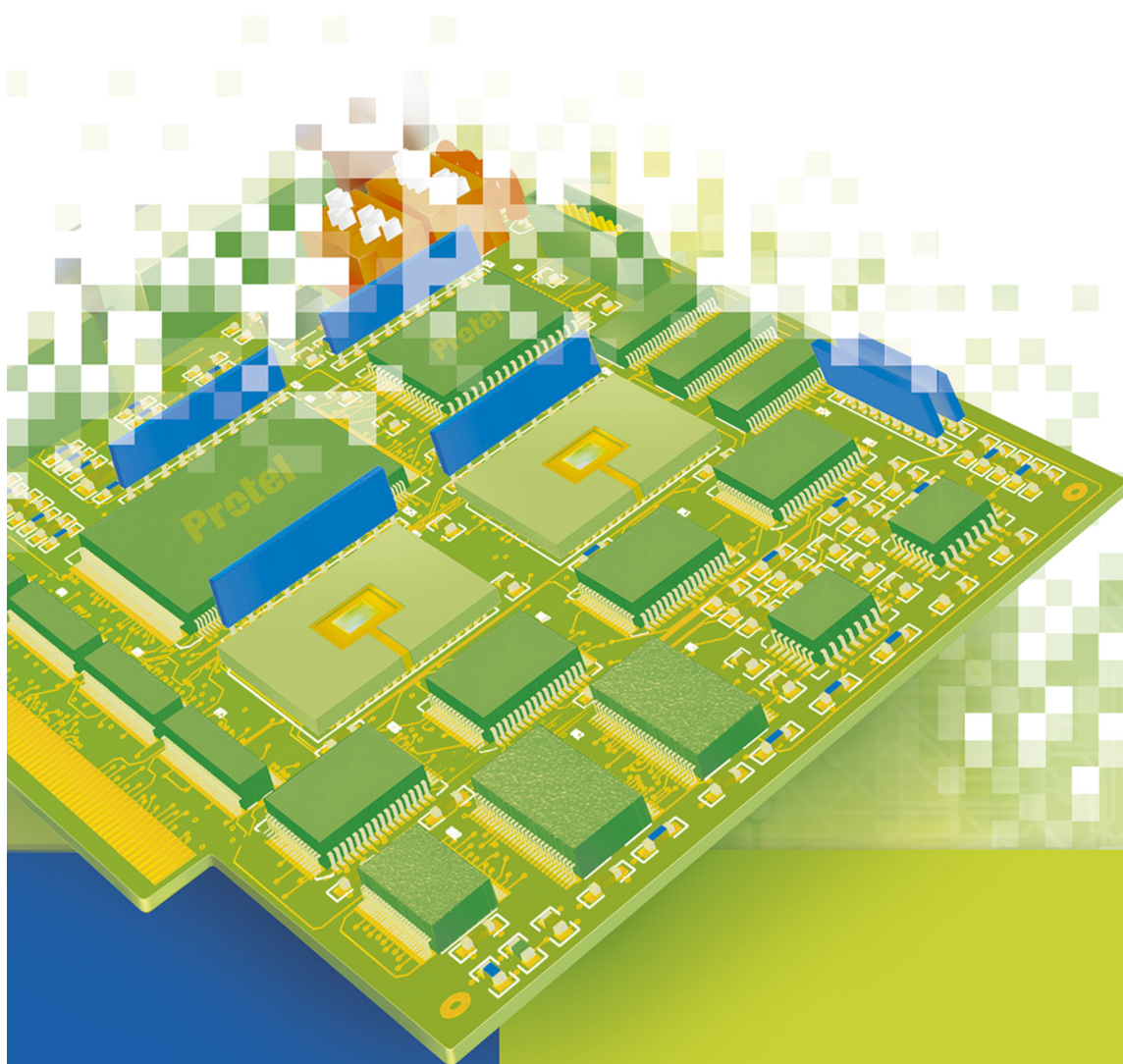


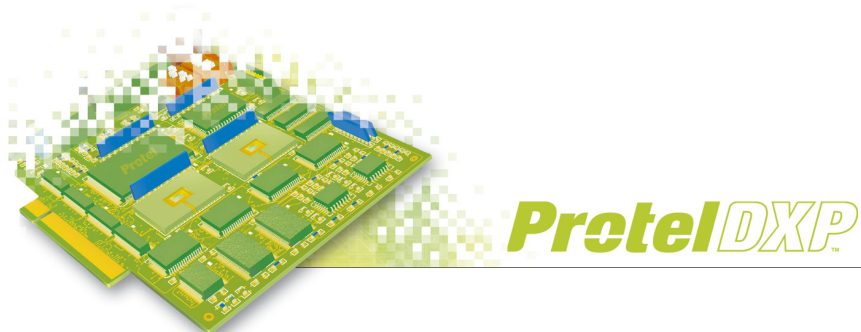
*Attributes for FPGA Devices*

**Protel**DXP™



**Protel**®

Board-level design system from Altium.



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## Attributes for FPGA Devices

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FPGA attributes are special directives that are used during the placement and routing of a FPGA design. They are used to control the linking of specialized components and utilize advanced features found on FPGAs. Typically attributes are placed in VHDL code or user constraint files and bear no meaning to any simulation outcome.

Protel DXP uses a unique way of placing attributes in your design by allowing users to directly place parameters in an intuitive design capture environment. Once placed, attribute information is automatically passed to the EDIF file allowing for easier integration and more rapid development of a system design using downstream tools.

Attributes listed here are dedicated for the DXP design capture system, however almost all attribute information from third party FPGA vendors can be used. More information on specialized attributes used on ports and components can be obtained from your FPGA vendors.

## Placing Attributes

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Attributes are placed on components and ports by using the **Parameters** tab found in the *Component Properties* and *Port Properties* dialogs respectively.

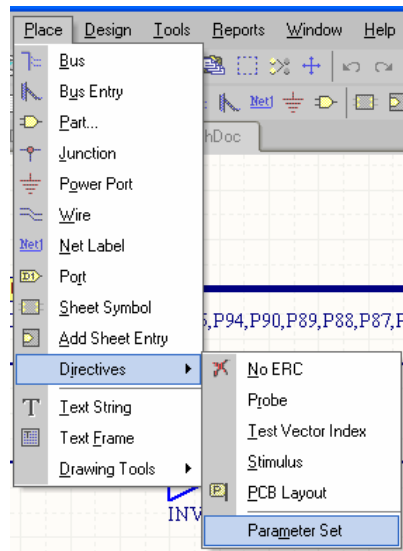
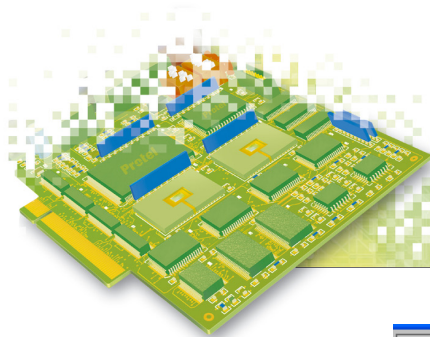
To place FPGA attributes, follow the steps below.

1. Display the *Properties* dialog by double-clicking on a port or schematic symbol and click on the **Parameters** tab.

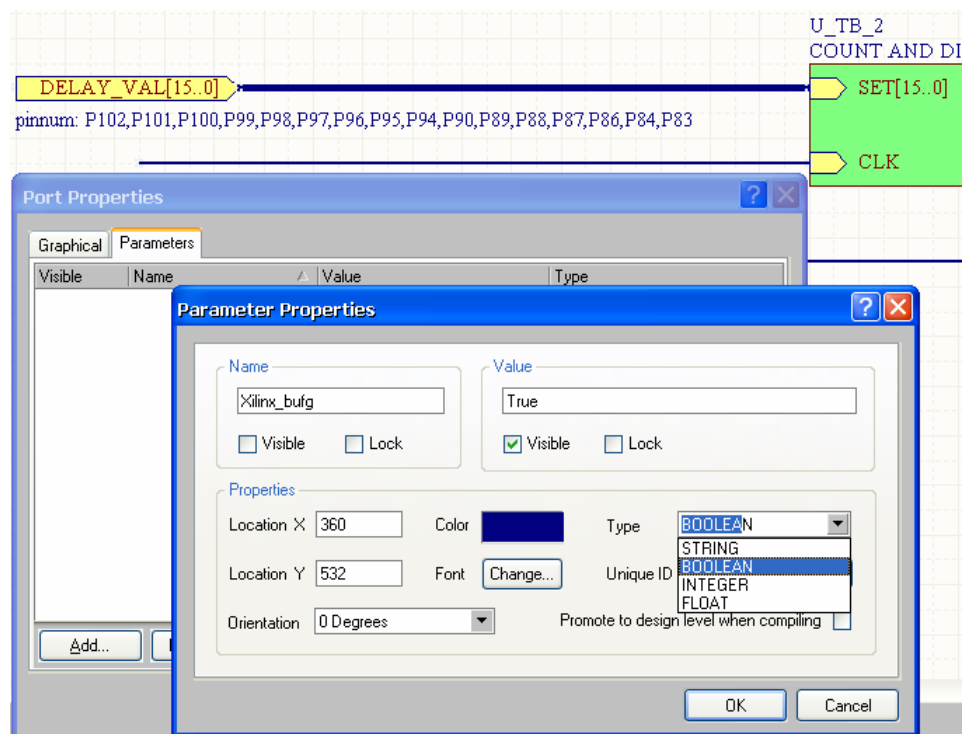
The project **Parameters** tab for adding FPGA target device information parameters is invoked by selecting **Project » Project Options** and selecting the **Parameters** tab.

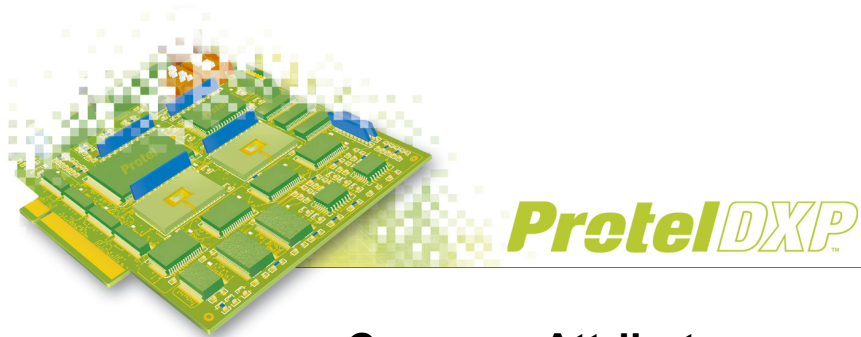
A schematic document's **Parameters** tab is accessed by invoking **Design » Options** and selecting the **Parameters** tab.

For wire or bus attributes, for example the Critical Path attribute, the information is placed through a Parameter Set object found by selecting **Place » Directive » Parameter Set**. Its *Parameters* dialog can be accessed by double-clicking on the placed Parameter Set object.



2. To add the attribute in the Parameters section, click on the **Add** button. This will bring up the *Parameters Properties* dialog.
3. In the Name and Value fields, provide the name and value of the attribute respectively. Change the Type to correspond with the attribute type.





## Common Attributes

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The common attributes are almost always used in the FPGA design flow. They are used to fix the target FPGA device and its pin locking information on a FPGA project.

### PIN Locking Attribute

The pin-locking attribute is used to lock the target device pins that are desired for signal and data processing. It is applied on ports in the top-level design unit.

Syntax for parameter properties:

Name: PINNUM

Type: STRING

Value: see below.

Bus port pins can be allocated the value of its FPGA pin by using (',') as a delimitator. These values are assigned to the elements of the port in a left to right order.

For example:

MY\_BUSPORT[7..0] bus port can have PINNUM attribute Value:

P1,P2,P3

The port is in descending order and any extra slices will be ignored. In this case MY\_BUSPORT7 port slice gets P1.

Another example is below:

MY\_BUSPORT[0..5] port can have PINNUM attribute value:

P1,P2,P3,P4,P5

This time the port is in ascending order so MY\_BUSPORT0 port slice gets P1 pin of the target device.

### Target Device Attribute

The target device attribute can be used to pass information for some place and route tool. The place and route tool automatically selects the target device part name from its own selection menu. The attribute can be placed to avoid manual selection of target device name each time the EDIF file is loaded for compiling into the FPGA vendor's place and route tool.

Syntax for parameter properties:

Name: PART\_NAME

Type: STRING

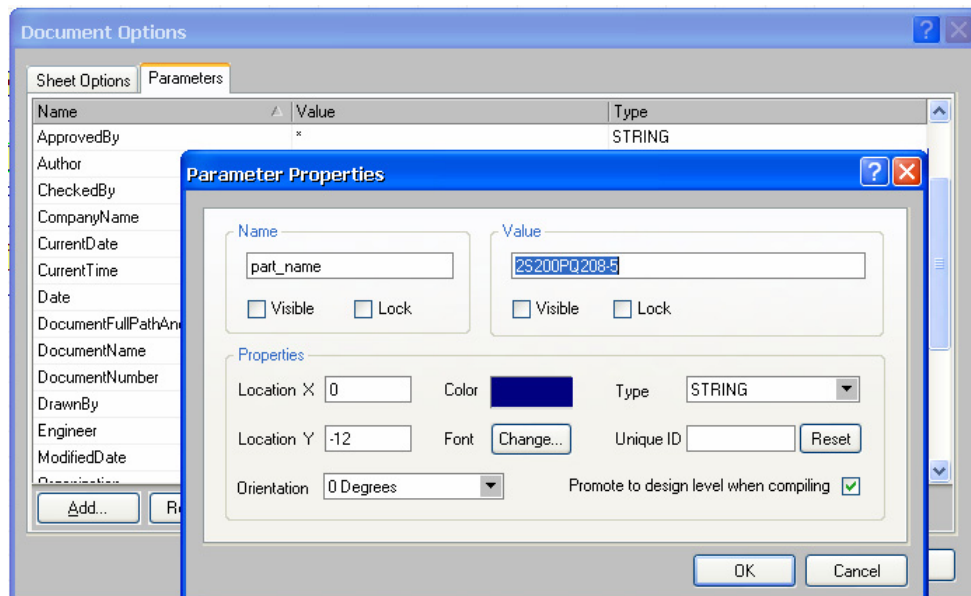
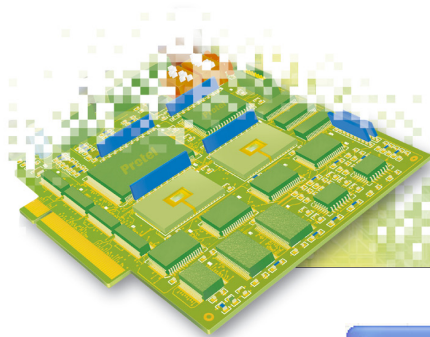
Value: see below.

For example, the heart monitor project's top-level unit would have the value:

2S200PQ208-5

The value of the particular target device can be obtained from the manufacturer's place and route tool.





## Advanced Attributes

The advanced attributes are used for optimizing the final outcome of the EDIF file. They also allow you to add information on selected ports and components. Advanced attributes include macrocell, critical path, inhibit\_buf, FPGA\_GSR and clock\_buffer attributes.

### Macrocell Attribute

The macrocell attribute is used on components that have EDIF macro files. It implies that the component is essentially a “black box” and should not be synthesized. It allows for the proper linking of the parent EDIF netlist output with the netlist from some other synthesis tools. By default, all components are assumed to be Macrocell, so this parameter is not generally required.

Syntax for parameter properties:

Name: MACROCELL

Type: BOOLEAN

Value: TRUE

### Critical Path Attribute

The critical path attribute allows the user to select a wire on the schematic whose timing is critical. Since the synthesis tools add factoring on signals (wires), this causes time delay. The use of this attribute allows you to have control on factoring of signals (wires) in your design. To place this attribute, select **Place » Directive » Parameter Set** menu and add the attribute parameter as described in the *Placing Attributes* section of this tutorial.

Syntax for parameter properties:

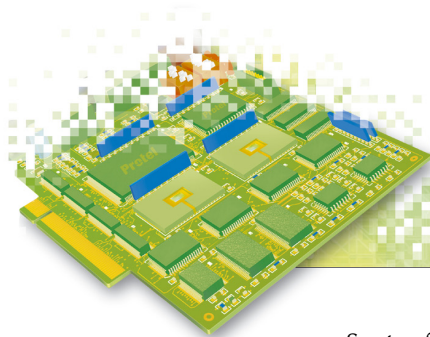
Name: CRITICAL

Type: BOOLEAN

Value: TRUE

### Inhibit\_buf Attribute

The inhibit\_buf attribute is used on selected ports to disable the insertion of I/O buffers if the “EDIF for FPGA” generators **Insert I/O Buffers** is turned on.



Syntax for parameter properties:

Name: INHIBIT\_BUF

Type: BOOLEAN

Value: TRUE

## FPGA\_GSR Attribute

If a FPGA design is compiled in several parts (and the EDIF linked later to another design) then the top-level must have a STARTUP (or equivalent) symbol and the other levels must have a FPGA\_GSR attribute attached to their RESET port.

When used, the marked port is disconnected from any flip-flop preset or clear and for Xilinx the flip-flop has an INIT properties added since some FPGAs have an active low GSR and require the appropriate signal in the VHDL be coded as active low.

A STARTUP for Xilinx device or equivalent for other vendor's symbol must be placed in the top level and connecting its GSR input to a port. If the whole design is compiled in one pass (regardless of the number of entities) then no FPGA\_GSR attribute is required.

Syntax for parameter properties:

Name: FPGA\_GSR

Type: BOOLEAN

Value: TRUE

## Clock\_Buffer Attribute

This attribute causes a clock buffer to be added in place of an input buffer when the EDIF for FPGA generators **Insert I/O Buffers** is selected. If buffers are not being inserted, the user may simply place a technology specific clock buffer symbol before the system clock port.

Syntax for parameter properties:

Name: CLOCK\_BUFFER

Type: BOOLEAN

Value: TRUE

## Technology Specific Attributes

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### Attributes for Xilinx Flavor EDIF output

#### 1. Xilinx\_GSR attribute

Same as FPGA\_GSR but specific for Xilinx technology.

Syntax for parameter properties:

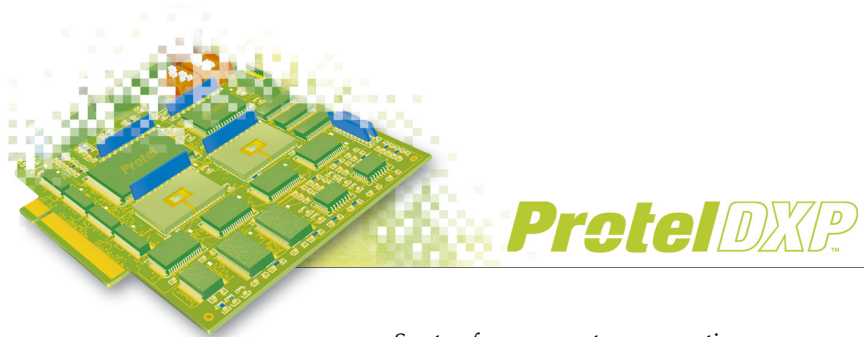
Name: Xilinx\_GSR

Type: BOOLEAN

Value: TRUE

#### 2. Xilinx\_BUFG attribute

This attribute adds a dedicated component on a system clock port. It also is used to override insertion of a general pad on a selected port when **Insert I/O Buffers** is ticked on. This attribute must be used only on global system clock ports.



Syntax for parameter properties:

Name:       Xilinx\_BUFG

Type:        BOOLEAN

### Other Attributes

The Protel DXP design capture system supports almost all attribute information provided by FPGA vendors and these attributes can be placed in the exact same manner. For example, the attributes for Xilinx FPGA technology, such as INIT (component initialization attribute used on LUT, ROM, FF, etc.) or RLOC (RLOC attribute constraint groups logic elements into discrete sets), can be placed following the steps described in the *Placing Attributes* section of this tutorial. The Type must be chosen to match as described in vendor-provided attribute or VHDL directive documents.