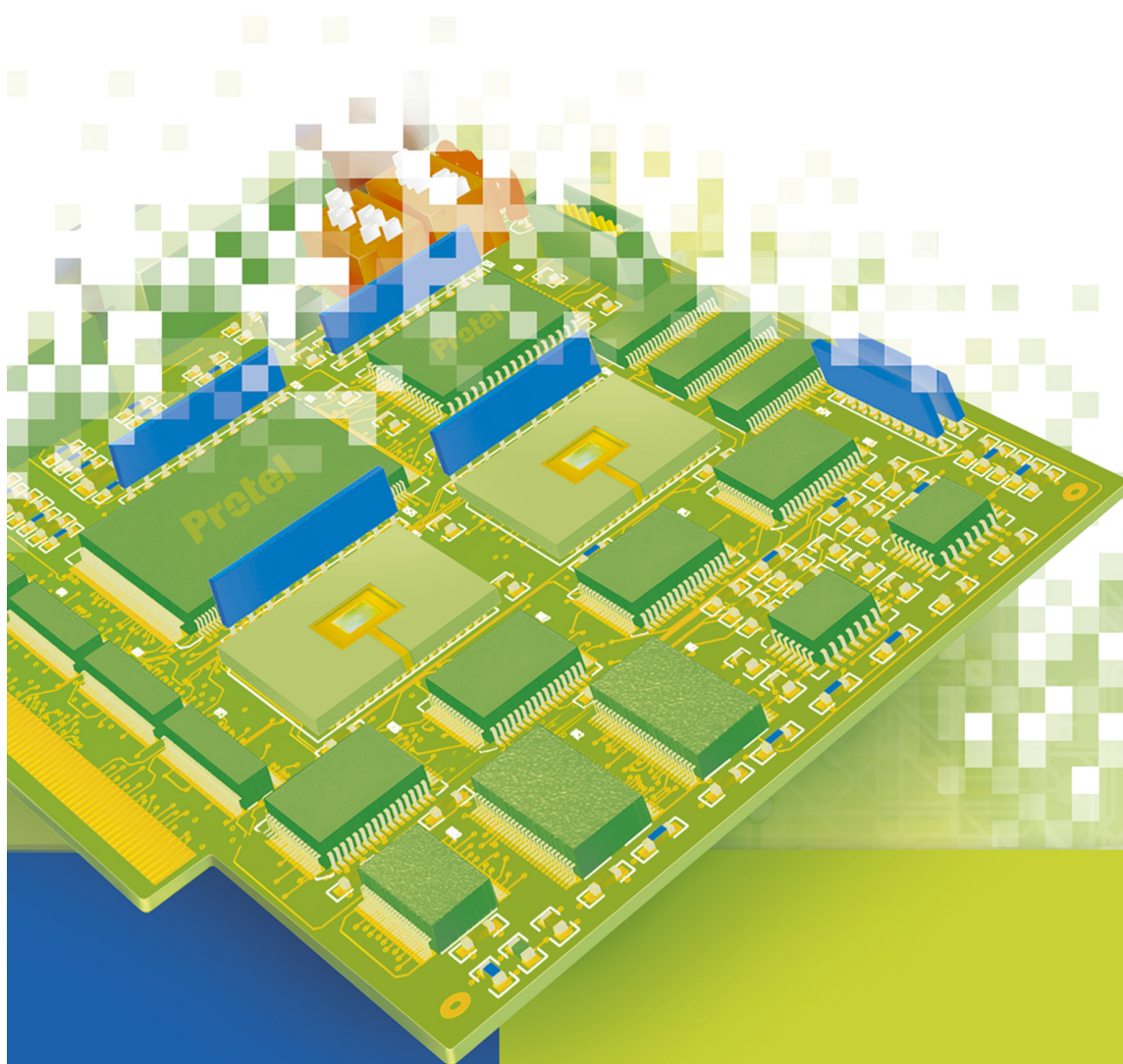


## *Protel DXP & Altera Interface*

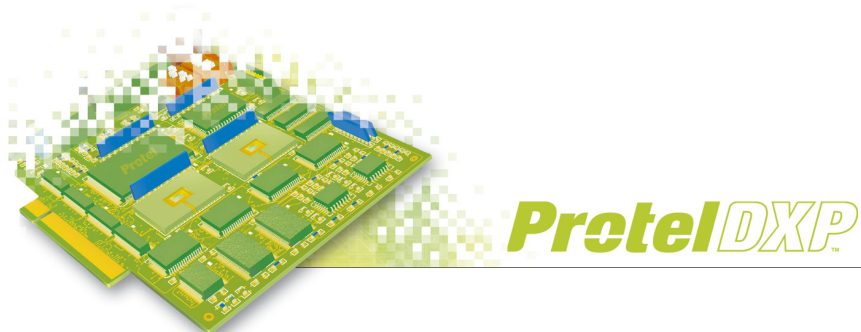
# **Protel**DXP™

## Tutorial



# **Protel**®

Board-level design system from Altium.



## Table of Contents

---

Protel DXP & Altera Interface .....	2
Altera Integrated FPGA Library.....	2
Altera Integrated PCB Library .....	2
Supported Libraries.....	2
Placing Common Attributes .....	3
Importing EDIF .....	3
Importing EDIF in Max+Plus-II .....	3
Importing EDIF in Quartus.....	5

## Protel DXP & Altera Interface

---

Altera FPGA programming design can now be created easily using the schematic entry method and the Altera integrated schematic FPGA library.

This tutorial will guide you with the necessary steps needed to start creating FPGA designs for programming Altera FPGA devices. By using the EDIF for FPGA schematic translator and the Altera library mapping file (LMF), your design can be routed and successfully downloaded on to a chip using the placement and routing tools available from Altera.

## Altera Integrated FPGA Library

---

The Altera integrated schematic library includes the most common primitives and old style TTL macro components ready for placement in your design.

The components in the library are grouped by functionality and type. Common functions can easily be found using sort by source.

The integrated schematic library package includes the library-mapping file (LMF). This is provided for integrating and routing the generated EDIF file with the Altera placement and routing tools.

## Altera Integrated PCB Library

---

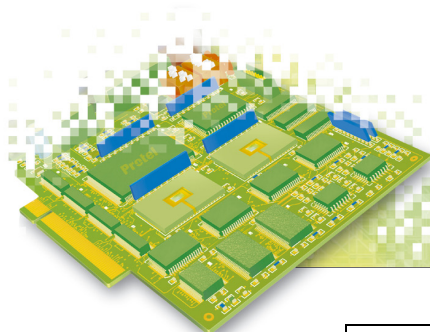
There is a range of schematic PCB design libraries available to support your PCB design needs using Altera devices.

## Supported Libraries

---

This table shows the supported items that are included in Protel DXP. For update information and library needs, please contact your ATS representative.

Technology	EDIF Support	FPGA Library	PCB Library
Stratix	Yes	Altera FPGA	PLD Stratix
Apex 20K	Yes	Altera FPGA	PLD Apex 20K
Apex 20KE	Yes	Altera FPGA	PLD Apex 20K
Flex 10K/A/B/E	Yes	Altera FPGA	PLD Flex



Technology	EDIF Support	FPGA Library	PCB Library
Flex 6000	Yes	Altera FPGA	PLD Flex
Flex 8000	Yes	Altera FPGA	PLD Flex
Acex 1k	Yes	Altera FPGA	PLD Acex 1k
Max 3000A	Yes	Altera FPGA	PLD Max 3000
Max 5000/A	Yes	Altera FPGA	PLD Max 5000
Max 7000/A/E/S/AE	Yes	Altera FPGA	PLD Max 7000
Max 9000/A	Yes	Altera FPGA	PLD Max 9000
Classic	Yes	Altera FPGA	PLD Classic EP
Apex II	Yes	Altera FPGA	Contact ATS
Apex 20KC	Yes	Altera FPGA	Contact ATS
Mercury	Yes	Altera FPGA	PLD Mercury

## Placing Common Attributes

Common attributes can be placed for recognition by the Altera's placement and routing tools. Placing common attributes will eliminate extra time required to configure the placement and routing tools each time your design is compiled.

To place pin lock information, use the values defined in the data sheet of your target device. For example use type 1, 2, 3 in the value field when you define the **pinnum** attribute.

The attributes are automatically passed to the ACF and the TCL files used during compilation in **Max+Plus-II** and **Quartus** place and routing environments respectively.

## Importing EDIF

To download your design on to a chip, more advanced tutorials and documents are available from Altera. These steps are provided to get you quickly started with routing and downloading your design on to an FPGA device.

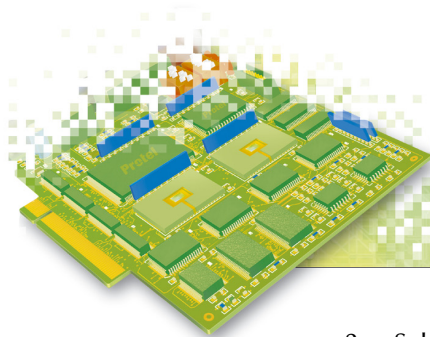
Once you have created your design using the Altera FPGA library and have invoked the EDIF for FPGA netlist, check your project output folder that must contain EDF, ACF and TCL files. These files must be present in the directory where you wish to import and compile your design using the placement and routing tools.

To compile your EDIF file for downloading onto the chip, you must use the LMF file available in the Program Files\Altium\Library\EDIF\ folder and use the 'Custom' EDA/Tool Vendor setting.

### Importing EDIF in Max+Plus-II

The Max+Plus-II package allows you to exploit the power of MAX, FLEX and ACEX devices. Following these steps will enable you to quickly get started with importing your EDIF with Max+Plus-II routing solution.

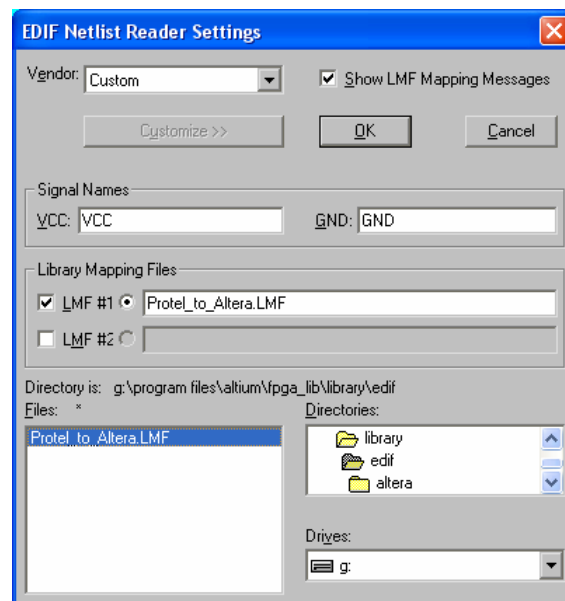
1. Insure that your compilation folder contains the EDF and the ACF file. Open the EDIF file by selecting **File » Open** from the menus. Browse and select the top-level EDIF file from your project output directory. Insure that there is no space in the design path to avoid potential errors during loading and routing.



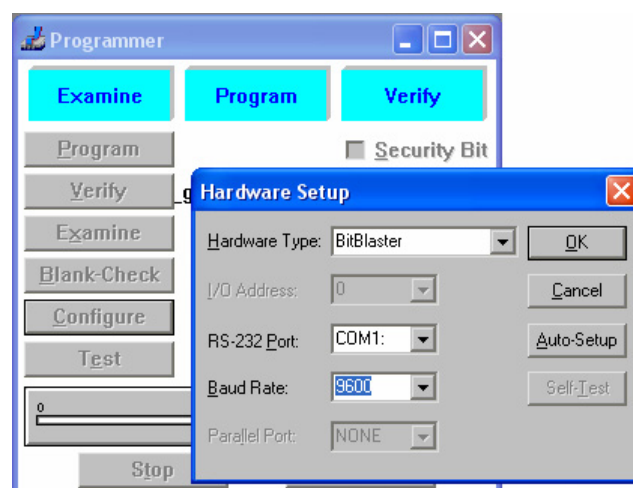
2. Select **File » Project** from the menus and then select **Set Project to Current File**.
3. Select **MAX+Plus-II » Compiler** from the left hand side of the menu bar. This will change the menu bar to now include compiler drop down menus.
4. To set the LMF, click on **Interfaces** and select **EDIF Netlist Reader Settings**.

For the Vendor, choose **Custom** and click on **Customize >>**.

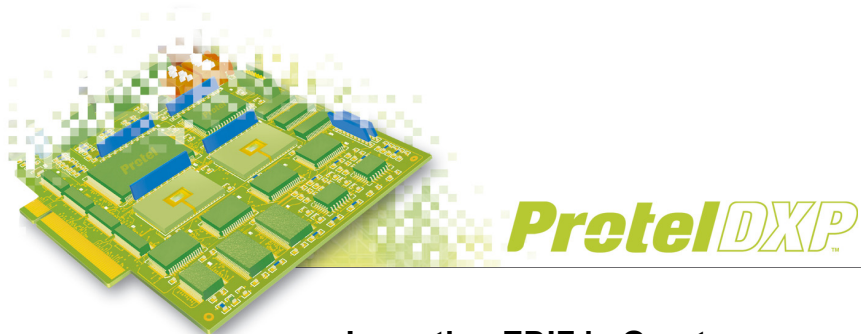
In the Customize section, place the net name you used in your schematic environment to define GND and VCC levels. In the Library Mapping Files section, tick on **LMF#1** or **LMF#2** and set directory path to the `Protel_to_Altera.lmf` file.



5. Choose the device and pin location from the **Assign** menu if not already set as attributes in the Protel DXP environment.
6. Click on **Start** to compile your design.
7. Insure that you have installed the system drivers for your download hardware type.
8. Bring up the programming menu by selecting **MAX+Plus II » Programming**. Configure your Hardware Setup and download the program onto the chip.





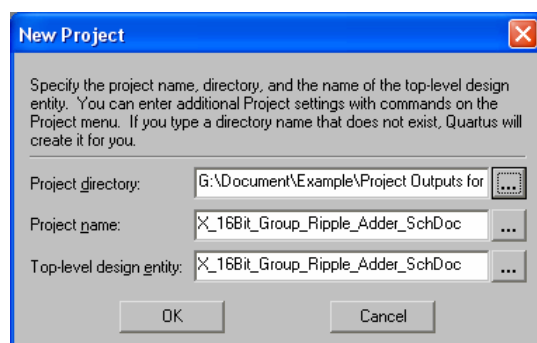


## Importing EDIF in Quartus

The Quartus routing solution allows you to exploit the power of APEX devices. Following these steps will enable you to quickly get started with routing and downloading your design.

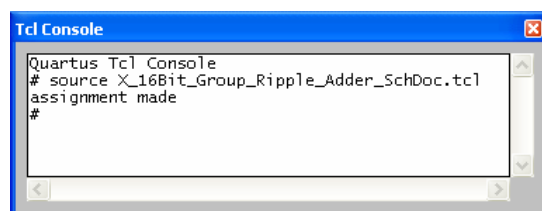
1. Select **File » New** and from the dialog and the **Project Files** tab, choose **Project File**.
2. In the *New Project* dialog, indicate the Project directory by opening the EDIF file in your planned compilation directory. The TCL file must be present in this directory.

For the **project name** and **Top-level design entity** fields, values should be automatically inserted after opening the EDIF file.



3. Bring up the TCL Console window by selecting **View » Auxiliary Windows**.
4. In the Quartus TCL console window, type `source <design_name>.tcl`.

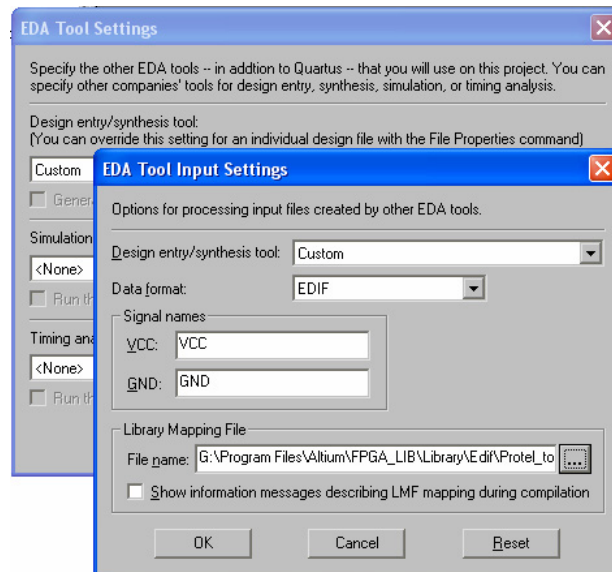
The design\_name is the same as the name of the EDIF file generated from Protel DXP environment.



5. To set the LMF file, select **Project » EDA Tool Settings**.

Go to the **Design entry/synthesis tool:** pull-down menu and select **Custom**. Click on **Settings** to bring up the *EDA Tool Input Settings* dialog.

Set **Data format** to **EDIF** and place your defined power net names if used in your schematic design. In the Library Mapping File section, set the path to the LMF file.



6. Select **Processing » Compiler Settings**. Set your FPGA device and other options from the various tabs available.
7. Select **Processing » Start Analysis & Elaboration**.
8. Select **Processing » Start Compilation**. Note any important information generated in the message output box.
9. Analyze the information available from the Compilation Report hierarchy tree and re-set options as needed.
10. Select **Processing » Open Programmer**. Configure your desired mode and set your Programming Hardware type. Add your programming file and device. Initiate downloading by clicking on **Start**. Note that jam and jvc files can be generated from the **Tools** menu.