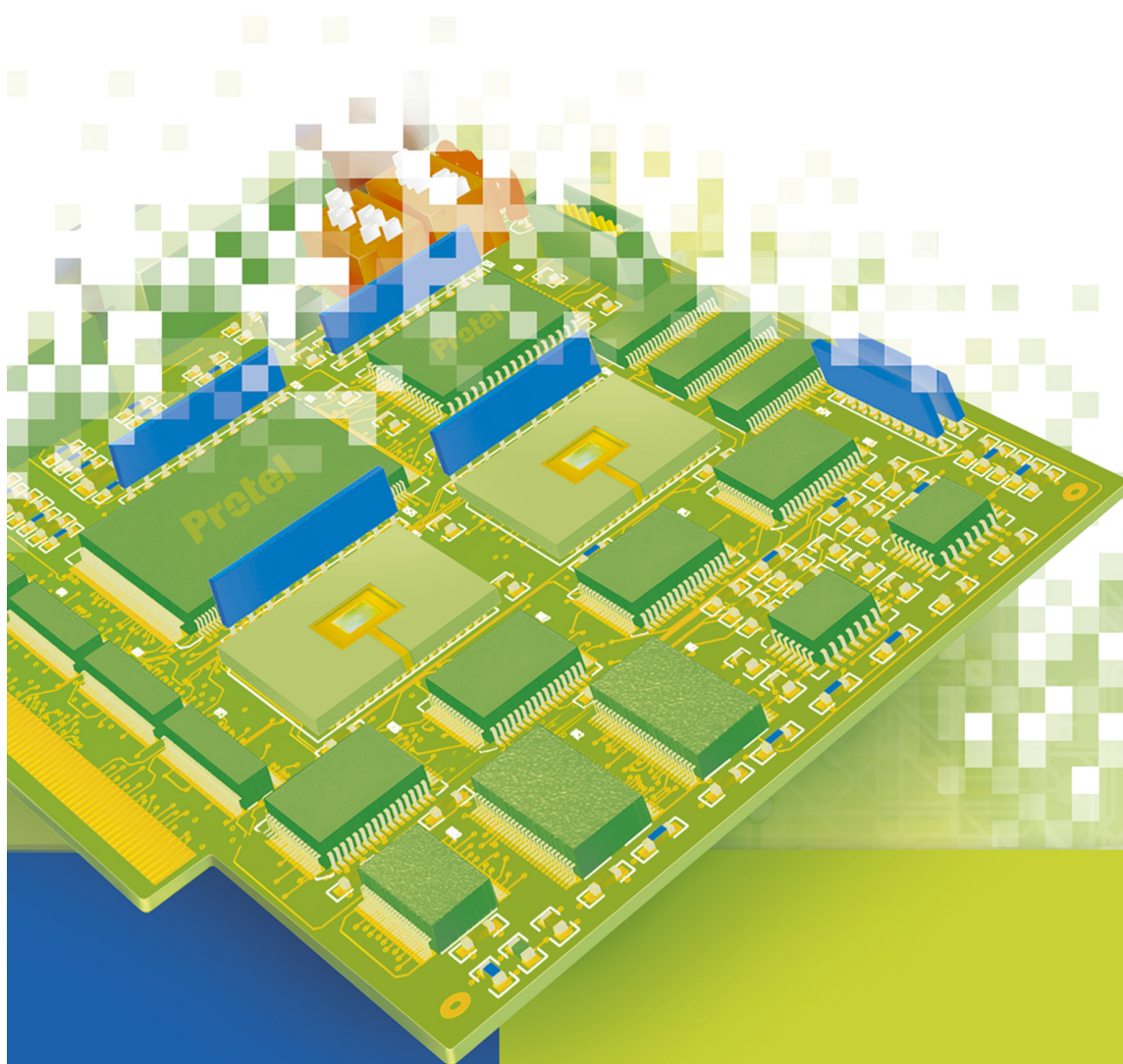


Protel DXP & Xilinx Interface

ProtelDXP™

Tutorial



Protel®

Board-level design system from Altium.

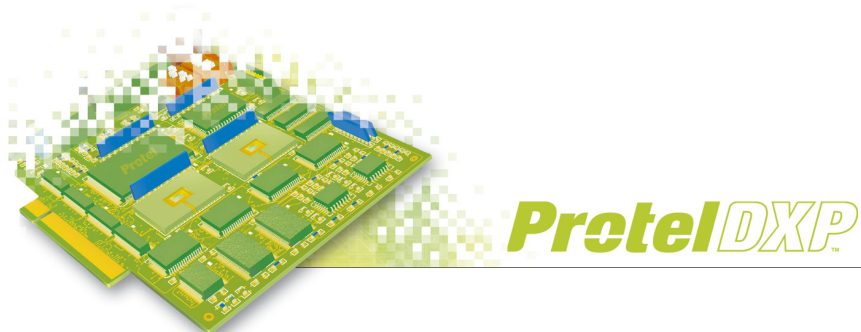


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Protel DXP & Xilinx Interface

This tutorial explains the Xilinx FPGA schematic library and other important information that will enable you to start using Protel DXP for programming Xilinx FPGA device with placement and routing tools. Instructions here will get you started with importing your design EDIF file into the Xilinx *Design Manager* Placement and routing tool.

The Xilinx FPGA integrated library and tutorial here are based on the *Xilinx Libraries Guide*, available in ISE 4.1 and 4.2 place and route tools.

Protel DXP comes with range of libraries and features that enable you to begin programming FPGAs in an intuitive schematic environment.

Xilinx Integrated Architecture FPGA Library

Xilinx FPGA integrated library package includes all the necessary symbols used for schematic design entry. The integrated libraries contain both the Unisim and Macro types of components.

Unisim libraries are a set of supported components that are pre-built on FPGA devices. Typically gate level components are available in all FPGA devices; however, some devices support more advanced level components.

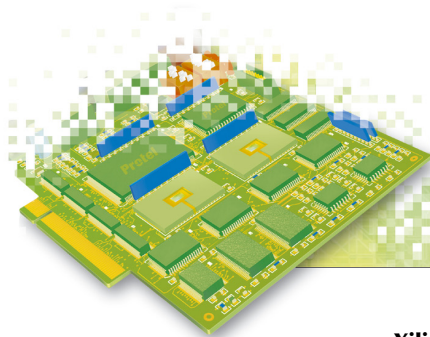
Some FPGA devices do not come with many of the pre-built components and therefore, to support such components, they are defined using gate level components. These types of elements are called *macro components*. Sometimes macro components are also used to define other higher-level function circuits. The uses of these macro components in your design allow efficient use of onboard FPGA device resources.

The macro component design file is delivered in EDIF. If they are used in your schematic design, their respective EDIF file must be present in your placement and routing directory to successfully download on to the chip.

Architecture specific integrated libraries are packaged according to the selection guide provided in the *Xilinx Libraries Guide*. This insures that only specific components that are available with your target device are used in your design. Specific notes on some specialized components are also available in *Component Properties* dialog.

The libraries include:

- **Xilinx Spartan FPGA.INTLIB**
This library is used for programming Spartan family XC2S* devices.
- **Xilinx Spartan-XL FPGA.INTLIB**
This library is used for programming Spartan family XCS*XL devices.



- **Xilinx Spartan-II & Spartan-IIE FPGA.INTLIB**

This library is used for programming Spartan-II and Spartan-IIE family of devices.

- **Xilinx Virtex & VirtexE FPGA.INTLIB**

This library is used for programming Virtex family XCV*, Virtex-E and Virtex-EM families XCV*E devices.

- **Xilinx Virtex-II & Virtex-II PRO FPGA.INTLIB**

This library is used for programming Virtex-II and Virtex-II PRO families XC2V* devices.

- **Xilinx CoolRunner-II FPGA.INTLIB**

This library is used for programming CoolRunner-II family of devices.

- **Xilinx CoolRunner-XPLA3 FPGA.INTLIB**

This library is used for programming CoolRunner-XPLA3 family of devices.

- **Xilinx XC4000E FPGA.INTLIB**

This library is used for programming XC4000E and XC4000L family of devices

- **Xilinx XC4000X FPGA.INTLIB**

This library is used for programming XC4000EX, XC4000XL and XC4000XLA family of devices.

- **Xilinx XC9500 FPGA.INTLIB**

This library is used for programming XC9500, XC9500XL and XC9500XV family of devices.

See the support table below for information on how these libraries are relevant to your Xilinx target device.

Xilinx LogiBLOX and Corelib FPGA Library

LogiBLOX is available as an accessory from Xilinx and allows you to generate your own specified component from a selection of common design module type. They are optimized for a particular FPGA architecture and are ready for instantiation in your design.

The LogiBLOX integrated schematic library contains most useful schematic symbols of components ready to be added into your schematic design. For more information, refer to the *LogiBLOX Guide*.

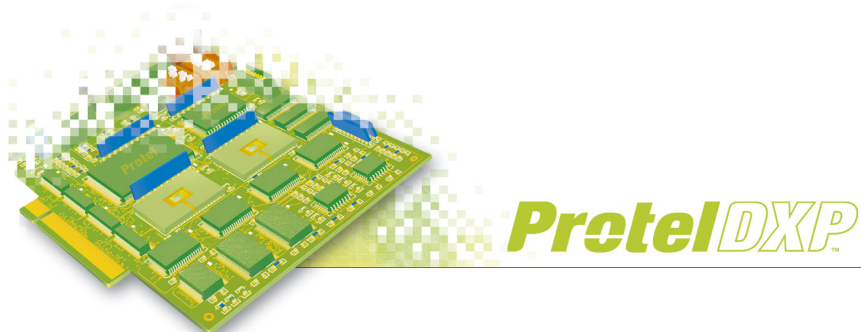
The CORE Generator System allows you to generate more complex IP modules such as Memory, Networking and Communication, and DSP core components. The generated EDIF files are also optimized for particular FPGA architectures. For more information, refer to the *CORE Generator System User Guide*.

Corelib integrated libraries contain parameterized schematic symbols of IP cores available from the CORE Generator System. To use them, you will need to modify their Library Ref and Comment fields from the *Component Properties* dialog and the Display Name and Designator fields from *Pin Properties* dialog.

To generate modules using LogiBLOX and Core Generator System, choose **Other** from the Vendor Name option and select **B<1>** from Bus Notation option.

Xilinx PCB Library

There is a range of schematic PCB design libraries available to support your PCB design needs using Xilinx devices.



Supported Libraries

This table shows the supported items that are included in Protel DXP release. For update information and library needs, please contact your ATS representative.

Technology	EDIF Support	FPGA Library	PCB Library
Spartan II E	Yes	Spartan-II & Spartan-II E	Spartan-II E
Spartan II	Yes	Spartan-II & Spartan-II E	Spartan-II
Virtex II Pro	Yes	Virtex-II & Virtex-II PRO	Virtex II Pro
Virtex II	Yes	Virtex-II & Virtex-II PRO	Virtex-II
Spartan	Yes	Spartan	Spartan
Spartan XL	Yes	Spartan-XL	Spartan XL
Virtex	Yes	Virtex & VirtexE	Virtex
Virtex E	Yes	Virtex & VirtexE	Virtex-E
CoolRunner II	Yes	CoolRunner-II	Contact ATS
CoolRunner XPLA3	Yes	CoolRunner-XPLA3	CoolRunner-XPLA3
XC9500	Yes	XC9500	PLD XC9500
XC9500XV	Yes	XC9500	PLD XC9500XV
XC9500XL	Yes	XC9500	PLD XC9500XL
XC4000E	Yes	XC4000 E	XC4000
XC4000EX	Yes	XC4000 X	Contact ATS
XC4000L	Yes	XC4000 E	Contact ATS
XC4000XL	Yes	XC4000 X	Contact ATS
XC4000XLA	Yes	XC4000 X	Contact ATS
XC4000XV	Yes	XC4000 X	Contact ATS

Xilinx Attributes

Xilinx FPGA attributes can be placed the same way as other attributes described in the *Attributes for FPGA Devices* document. For more detail information on Xilinx attributes, refer to the *Xilinx Libraries Guide*.

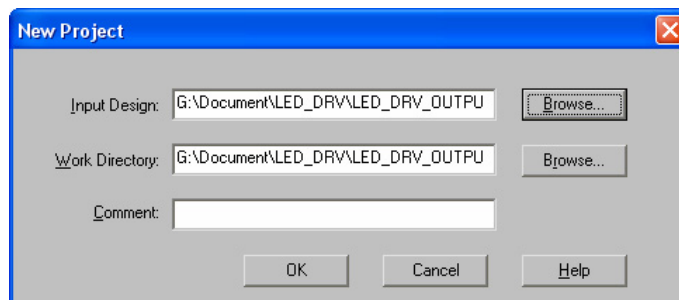
To place pin locking information, use the pin designator character found in your target device pin table documentation. For example, use **P<pin_number>** format to define pin location for a PQ208 package.

Importing EDIF

To import your EDIF file for placement and routing, use *Design Manager* available from Xilinx. This program can be invoked from **Program » Xilinx » Xilinx ISE4 » Accessories**. To download your program file on to the device, use *Impact* invoked from **Program » Xilinx » Xilinx ISE4 » Accessories**.

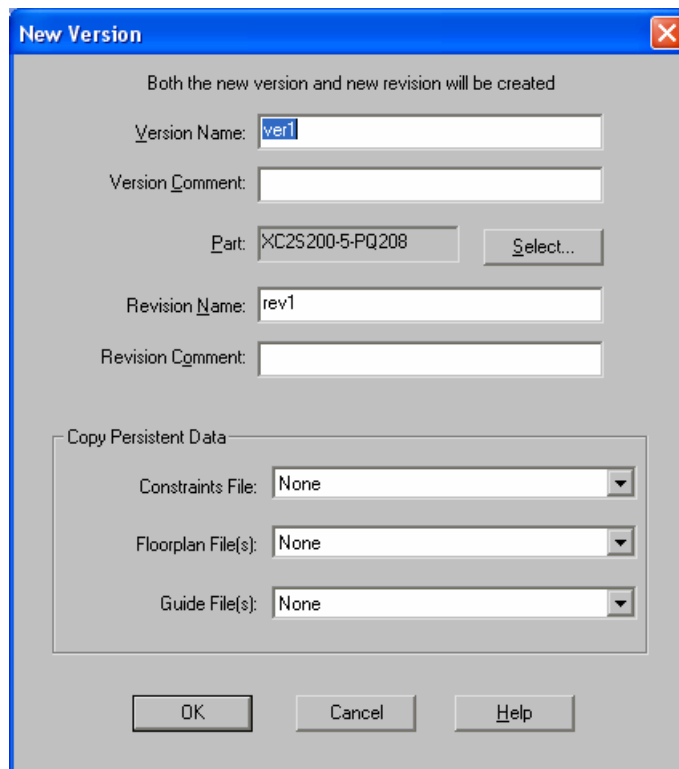
The instructions below describe how to import your EDIF file for routing and downloading on to a chip.

1. Select **File » New Project** from the menus.
2. In the *New Project* dialog, browse and open your top-level design EDIF file. Change the working directory or add a comment as necessary.



3. In the *New Version* dialog, note the Part information that may have been added in the schematic project using the **Target Device Attribute**. Correct Part information if necessary.

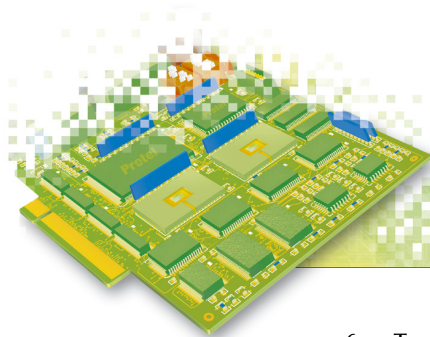
In the **Copy Persistent Data** section, you can also specify your UCF (User Constraint File). UCFs can be used to specify timing and other advanced attribute data to control your FPGA device. For more information on how to create a UCF file, refer to the *Xilinx Libraries Guide*.



4. Select **Design » Options** to add extra information or extracted simulation data during placement and routing of your design. Close the *Options* dialog and select **Design » Implement**.

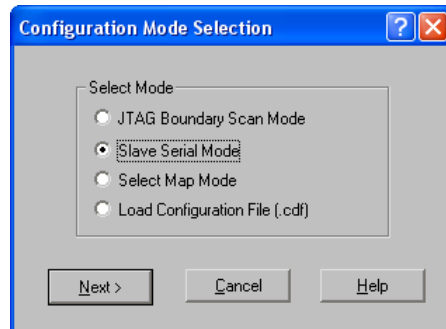
Note the new pop-up *Flow Engine* window that shows you the report and stage of your placement and route. This information is also available in the log report file.

5. Check you log file to see how much chip resources your design has taken. The log file also indicates warnings and errors that may have occurred during the routing process.

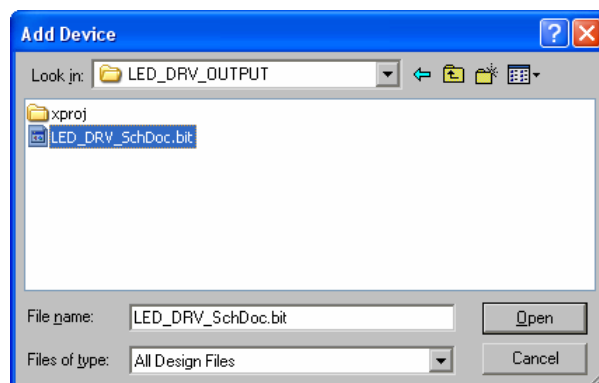


- To establish connection with your FPGA device, run the program 'Impact' from **Programs » Xilinx ISE 4 » Accessories**.

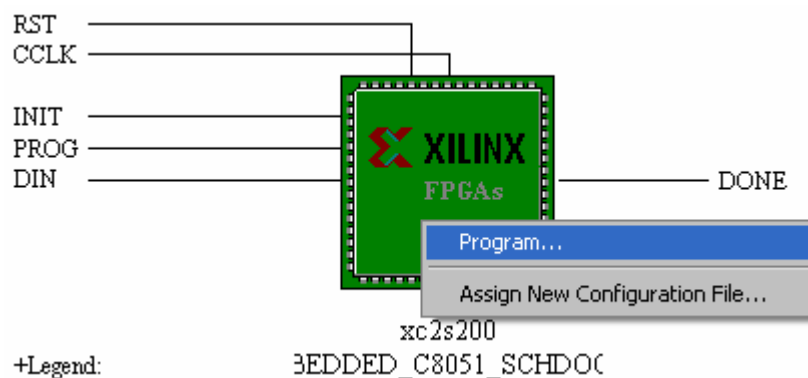
From the *Configuration Mode Selection* dialog, select the configuration mode to match your FPGA development board download configuration.



- Add the device configuration file by opening the BIT file. This is the Xilinx proprietary binary stream file that will get downloaded on to the chip for configuration. The file has the same top-level design name and it should be present in the directory where your EDIF file was loaded or the working directory.



- Initiate the download by right-clicking on the chip symbol and selecting **Program**.



- Your design is now downloaded on to the FPGA device.